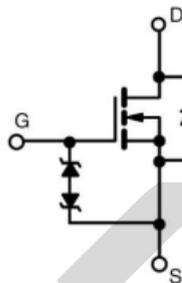


## N-Channel Super Junction MOSFET

**MCR60F075PT**

**TO-247**

**FRD MOSFET**  
**ESD protect**



$V_{DS}$	650	V
$R_{DS(on),TYP}$	75	m $\Omega$
$I_D$	42	A

### Features

- 1.Low on – resistance
- 2.Reduced Switching & Conduction Losses
- 3.Fast Recovery Body-Diode
- 4.Package TO-247

### Applications

- 1.PC power
- 2.Telecom power
- 3.Server power
- 4.EV Charger
- 5.Motor driver

**Maximum ratings, at  $T_A = 25^\circ\text{C}$ , unless otherwise specified**

### Absolute Maximum Ratings

PARAMETERS/TEST CONDITIONS	SYMBOL	LIMITS	UNITS
Drain-Source Voltage	$V_{DS}$	600	V
Drain Current –continuous @25°C	$I_D$	42	A
Drain Current –continuous @100°C	$I_D$	26.6	A
Pulsed Drain Current <sup>1</sup>	$I_{DM}$	126	A
Gate-Source Voltage	$V_{GS}$	$\pm 30$	V
Single Pulse Avalanche <sup>2</sup>	$E_{AS}$	254	mJ
Operating Junction & Storage Temperature	$T_j, T_{stg}$	-55 to 150	°C
Lead Temperature (1/16" from case for 10sec.)	$T_L$	260	°C

Note:

1. Pulse width limited by maximum junction temperature.
2.  $I_{AS} = 6.3\text{A}$ ,  $R_G = 25 \Omega$ , starting  $T_J = 25^\circ\text{C}$ .

## Electrical Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
--------	-----------	-----------	------	------	------	------

### Static Electrical Characteristics @ $T_j=25^\circ\text{C}$ (unless otherwise stated)

$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=1mA$	600	--	--	V
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS}=600V, V_{GS}=0V$	--	--	10	$\mu A$
	Zero Gate Voltage Drain Current ( $T_j = 125^\circ\text{C}$ )	$V_{DS}=480V, V_{GS}=0V$	--	--	30	$\mu A$
$I_{GSS}$	Gate-Body Leakage Current	$V_{DS}=0V, V_{GS}=\pm 30V$	--	--	$\pm 100$	nA
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=2.8mA$	3		5	V
$R_{DS(on)}$	Drain-Source On-State Resistance	$V_{GS}=10V, I_D=21.5A$	--	64	75	$m\Omega$

### Dynamic Electrical Characteristics @ $T_j = 25^\circ\text{C}$ (unless otherwise stated)

$C_{iss}$	Input Capacitance	$V_{DS}=400V, V_{GS}=0V, f=250KHz$	--	3080	--	$\mu F$
$C_{oss}$	Output Capacitance		--	83	--	$\mu F$
$C_{rss}$	Reverse Transfer Capacitance		--	2.4	--	$\mu F$
$Q_g$	Total Gate Charge	$V_{DS}=400V, I_D=21.5A, V_{GS}=10V$	--	76	--	nC
$Q_{gs}$	Gate-Source Charge		--	20	--	nC
$Q_{gd}$	Gate-Drain Charge		--	40	--	nC

### Switching Characteristics

$T_{d(on)}$	Turn-on Delay Time	$V_{DS}=400V, I_D=40A, R_G=2\Omega, V_{GS}=10V$	--	20	--	ns
$T_r$	Turn-on Rise Time		--	12	--	ns
$T_{d(off)}$	Turn-Off Delay Time		--	61	--	ns
$T_f$	Turn-Off Fall Time		--	7	--	ns

## Source- Drain Diode Characteristics@ $T_j = 25^\circ\text{C}$ (unless otherwise stated)

$I_s$	Continuous Current		--	--	42	A
$I_{SM}$	Maximum Pulsed Diode Forward Curren		--	--	126	A
$V_{SD}$	Forward Voltage	$V_{GS} = 0V,$ $I_{SD} = 21.5 A$	--	--	1.2	V
$T_{rr}$	Reverse Recovery Time	$V_{DS} = 400 V, I_{SD} = 21.5 A,$ $dI_F/dt = 100 A/\mu s$	--	134	--	ns
$Q_{rr}$	Reverse Recovery Charge		--	0.85	--	$\mu C$

NO COPY

## Typical Performance Characteristics

Figure 1. On-Region Characteristics

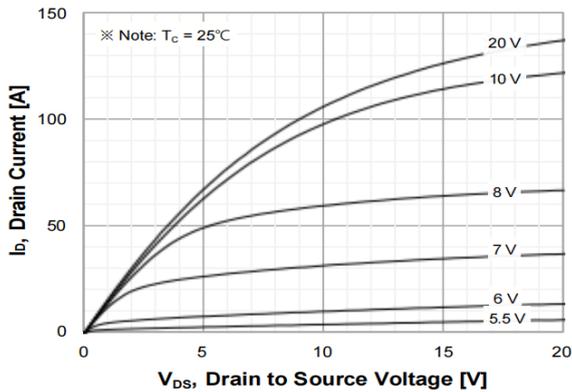


Figure 2. Transfer Characteristics

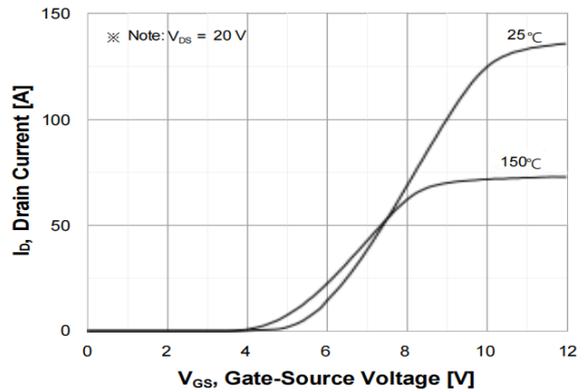


Figure 3. On-Resistance Characteristics vs. Drain Current and Gate Voltage

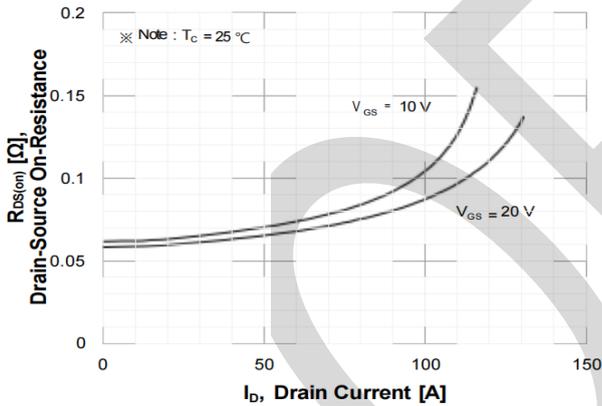


Figure 4. Diode Forward Voltage Characteristics vs. Source-Drain Current and Temperature

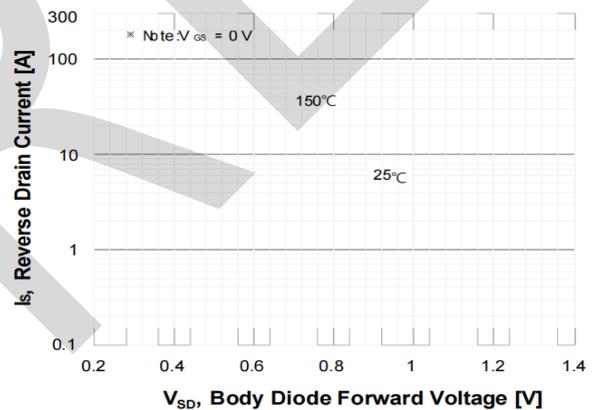


Figure 5. Capacitance Characteristics

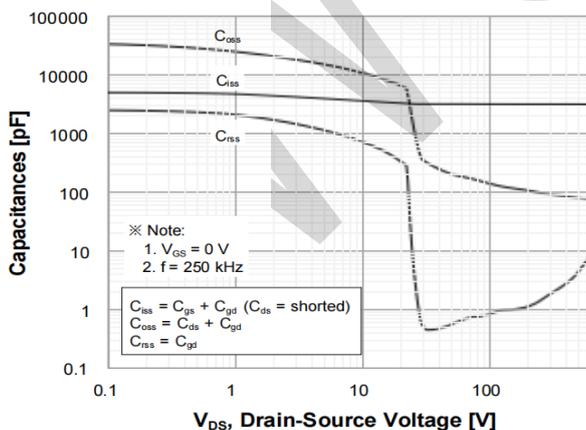
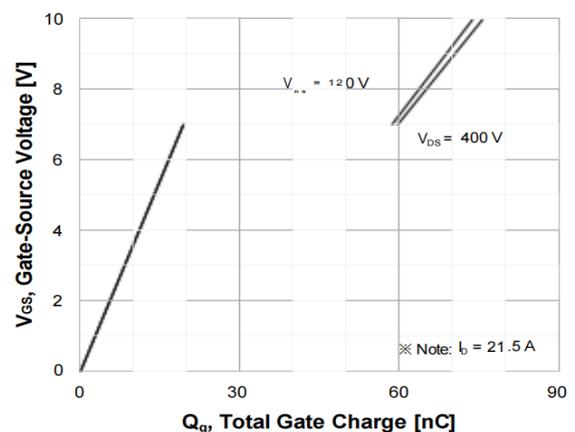
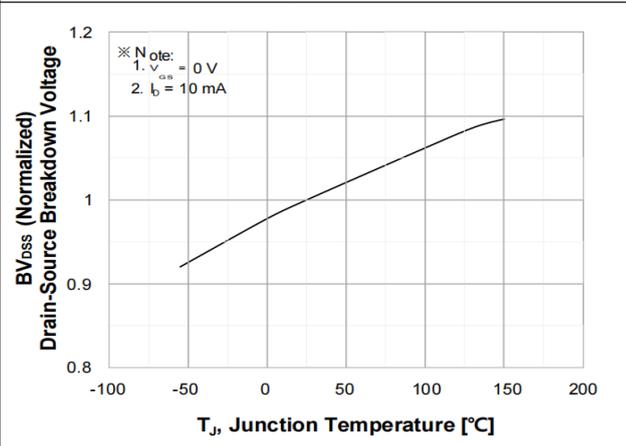


Figure 6. Gate Charge Characteristics

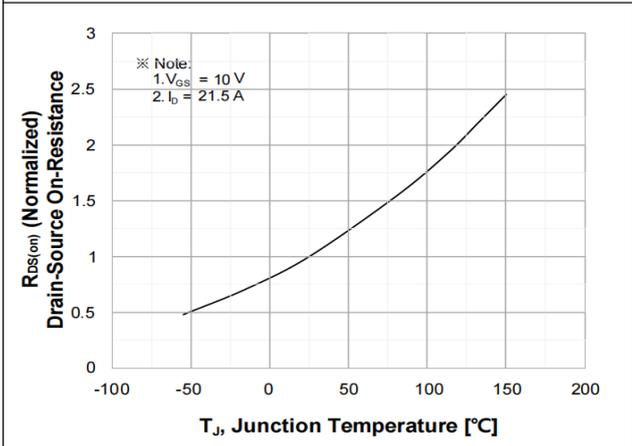


## Typical Performance Characteristics

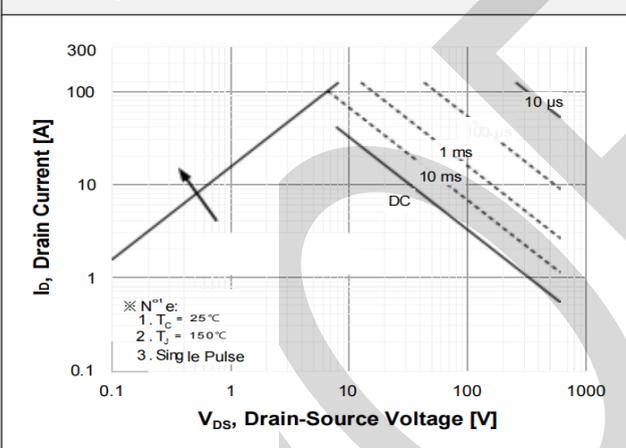
**Figure 7. Breakdown Voltage Characteristics vs. Temperature**



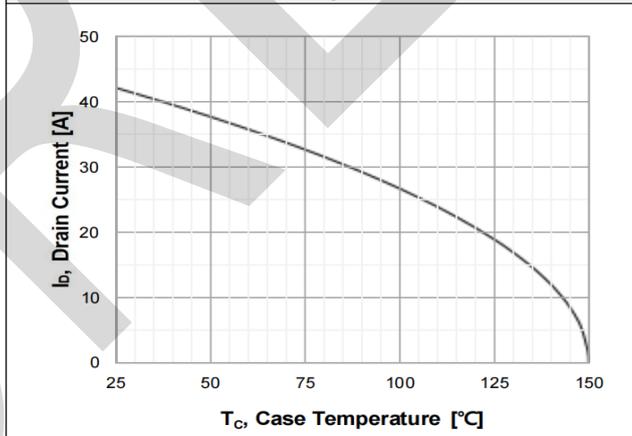
**Figure 8. On-Resistance Characteristics vs. Temperature**



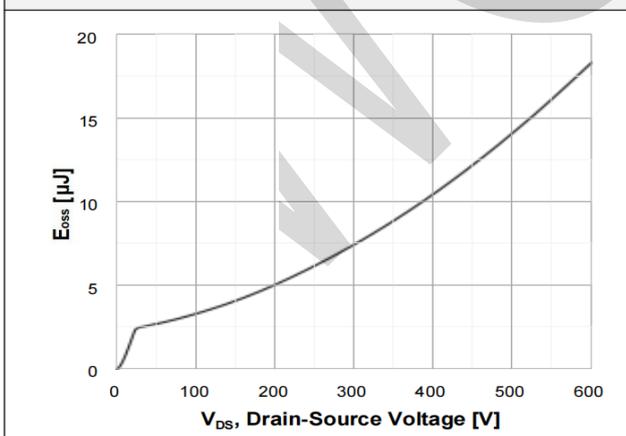
**Figure 9. Maximum Safe Operating Area**



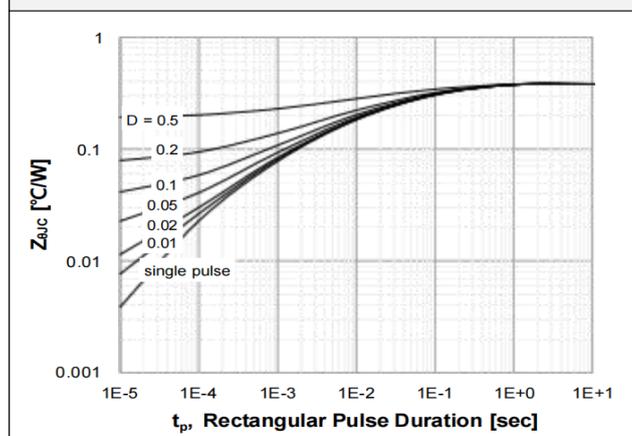
**Figure 10. Maximum Drain Current vs. Case Temperature**



**Figure 11. E\_OSS vs. Drain to Source Voltage**



**Figure 12. Transient Thermal Response Curve**



## Test Circuits

Figure 13. Inductive Load Switching Test Circuit and Waveforms

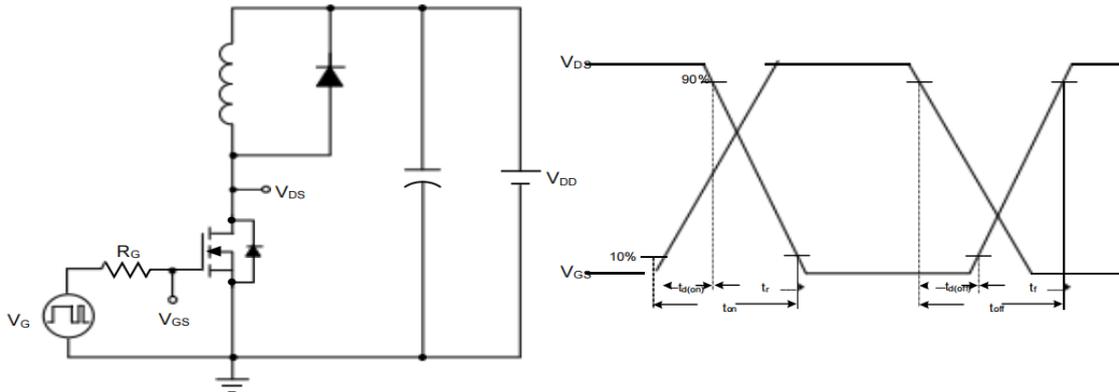


Figure 14. Unclamped Inductive Switching Test Circuit and Waveforms

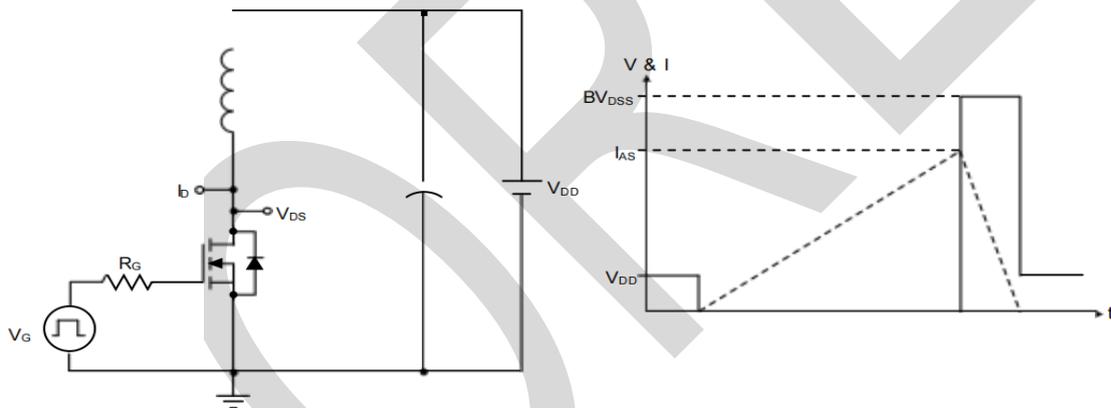
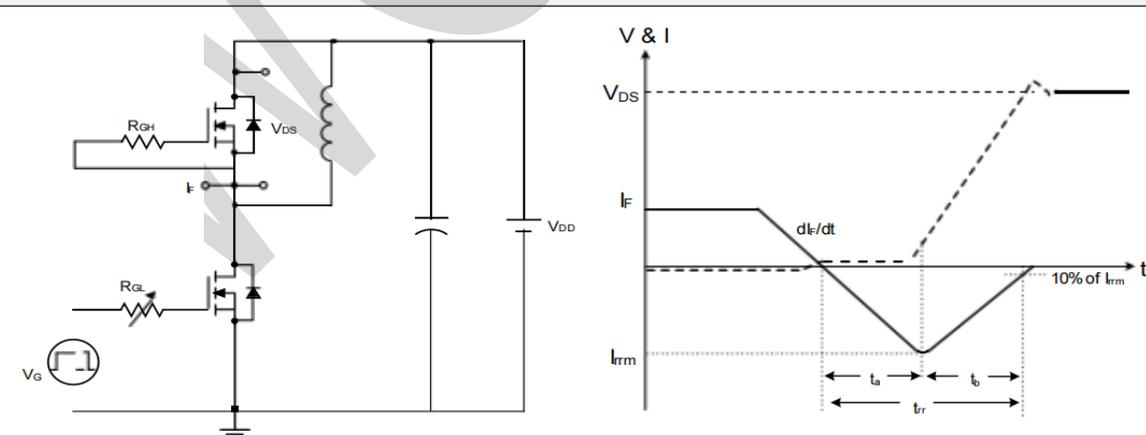
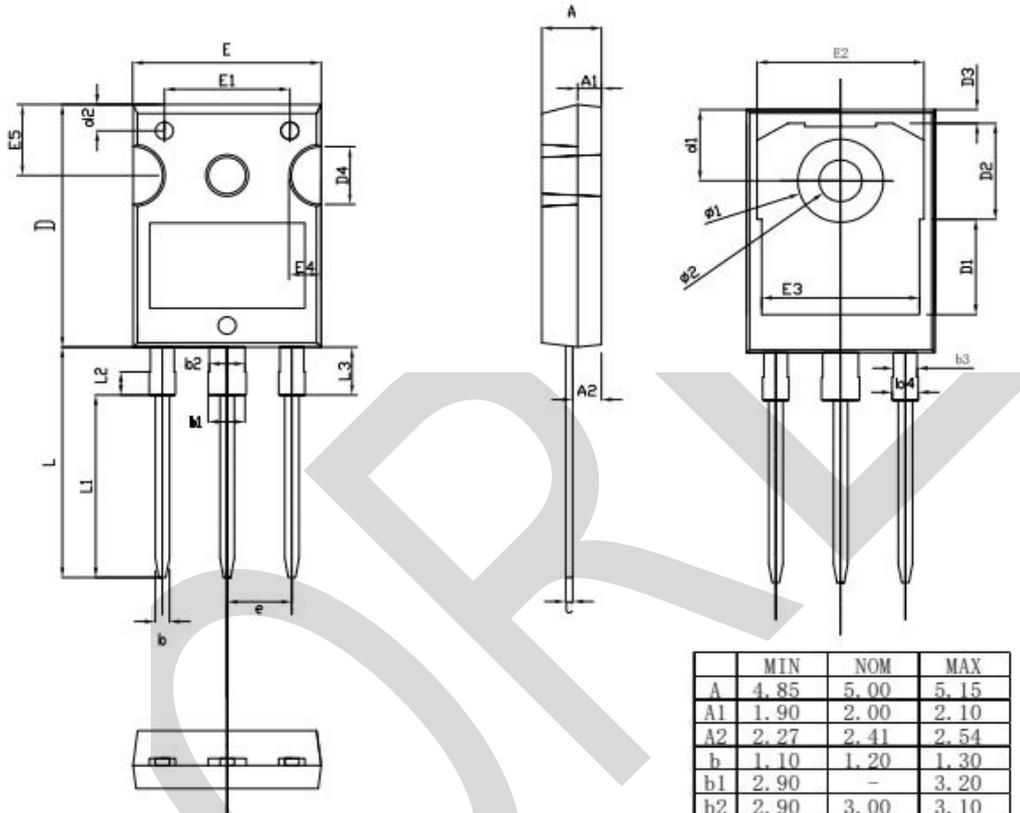


Figure 15. Peak Diode Recovery dv/dt Test Circuit and Waveforms

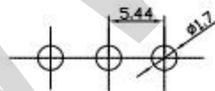


## PACKAGE OUTLINE DIMENSIONS

### TO-247



RECOMMENDED LAND PATTERN



UNIT: mm

	MIN	NOM	MAX
A	4.85	5.00	5.15
A1	1.90	2.00	2.10
A2	2.27	2.41	2.54
A3	2.27	2.41	2.54
b	1.10	1.20	1.30
b1	2.90	-	3.20
b2	2.90	3.00	3.10
b3	1.90	2.00	2.10
b4	2.00	-	2.20
c	0.55	0.60	0.68
D	20.80	21.00	21.10
D1	-	8.23	-
D2	-	8.32	-
D3	-	1.17	-
D4	3.68	4.90	5.10
d1	6.04	6.15	6.30
d2	2.20	2.30	2.40
E	15.70	15.80	16.00
E1	-	10.50	-
E2	-	14.02	-
E3	-	13.50	-
E4	2.20	2.40	2.60
E5	5.49	5.80	6.00
e	5.34	5.44	5.54
L	19.72	19.92	20.12
L1	-	15.79	-
L2	-	1.98	-
L3	4.00	4.10	4.47
phi 1	7.10	7.19	7.30
phi 2	3.50	3.60	3.70